IN THE CLAIMS:

New claims 7-14 have been added. Please note that all claims currently pending and under consideration in the referenced application are shown below. This listing of claims will replace all prior versions and listings in the application.

1. (Previously Presented) A method of forming a semiconductor device package, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, the active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of the plurality of individual die locations;

forming intermediate conductive elements over the plurality of bond pads to project a height above the active surface;

forming a pattern of mutually transverse channels in the active surface to a depth below the at least one layer of integrated circuitry, the channels circumscribing a semiconductor device location comprised of at least one individual die and exposing peripheral edges of the at least one layer of integrated circuitry;

applying an encapsulant material at least over the active surface and into the channels to a depth exceeding the height of projection of the intermediate conductive elements;

removing a depth of the encapsulant material sufficient to expose a portion of each of the intermediate conductive elements; and

placing the semiconductor substrate with the intermediate conductive elements in alignment with conductive bumps protruding from a carrier substrate; and

electrically connecting the intermediate conductive elements and the conductive bumps.

2. (Previously Presented) The method of claim 1, further including forming bond pads over the exposed portions of the intermediate conductive elements before electrically connecting the intermediate conductive elements to the conductive bumps.

3. (Withdrawn) A method of forming a semiconductor device package, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, the active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of the plurality of individual die locations;

forming intermediate conductive elements over the plurality of bond pads to project a height above the active surface;

forming a pattern of mutually transverse channels in the active surface to a depth below the at least one layer of integrated circuitry, the channels circumscribing a semiconductor device location comprised of at least one individual die and exposing peripheral edges of the at least one layer of integrated circuitry;

applying an encapsulant material at least over the active surface and into the channels to a depth exceeding the height of projection of the intermediate conductive elements;

removing a depth of the encapsulant material sufficient to expose a portion of each of the intermediate conductive elements; and

forming conductive traces over the encapsulant material from the exposed portions of the intermediate conductive elements to at least one channel of the pattern of channels, defining a peripheral edge of at least one individual die location of the plurality so as to define a plurality of laterally spaced edge contacts therealong, and severing the semiconductor substrate in alignment with at least some of the channels including the at least one channel into a plurality of semiconductor elements each comprised of the at least one individual die location, wherein the exposed peripheral edges of the at least one layer of integrated circuitry remain covered with the encapsulant material and the plurality of laterally spaced edge contacts are located along a peripheral edge of a semiconductor element of the plurality.

4. (Withdrawn) The method of claim 3, further comprising aligning the plurality of laterally spaced edge contacts with a plurality of edge connectors of a carrier substrate and electrically connecting the plurality of laterally spaced edge contacts with the plurality of edge connectors.

5. (Withdrawn) A method of forming a semiconductor device package, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, the active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of the plurality of individual die locations;

forming intermediate conductive elements over the plurality of bond pads to project to a peripheral edge of at least one individual die location of the plurality so as to define a plurality of laterally spaced edge contacts therealong;

forming a pattern of mutually transverse channels in the active surface to a depth below the at least one layer of integrated circuitry, the channels circumscribing the at least one individual die location and exposing the laterally spaced edge contacts of the peripheral edge;

applying an encapsulant material at least over the active surface and into the channels to a depth covering the intermediate conductive elements; and

severing the semiconductor substrate in alignment with at least some of the channels into a plurality of semiconductor elements each comprised of the at least one individual die location, wherein the plurality of laterally spaced edge contacts are exposed along the peripheral edge of the at least one individual die location.

6. (Withdrawn) The method of claim 5, further comprising aligning the plurality of laterally spaced edge contacts with a plurality of edge connectors of a carrier substrate and electrically connecting the plurality of laterally spaced edge contacts with the plurality of edge connectors.

7. (New) The method of claim 1, further comprising forming the channels with sloped side walls defining opposing chamfers.

8. (New) The method of claim 1, further comprising forming the channels with substantially parallel side walls.

9. (New) The method of claim 1, wherein forming the intermediate conductive elements is effected by forming at least one solder ball.

10. (New) The method of claim 1, wherein forming the intermediate conductive elements is effected by forming at least one pillar of a conductive or conductor-filled epoxy or a metal-filled elastomer.

11. (New) The method of claim 1, wherein forming the intermediate conductive elements is effected by a wire bonding capillary.

12. (New) The method of claim 1, wherein applying an encapsulant material comprises applying an encapsulant material of a material selected from the group comprising filled polymers, epoxies, silicones, silicone-carbon resins, polyimides, polyurethanes and glasses.

13. (New) The method of claim 1, further comprising applying another layer of encapsulant material on a back side of the semiconductor substrate.

14. (New) The method of claim 1, further comprising severing the semiconductor substrate along the pattern of mutually transverse channels into a plurality of semiconductor elements, each semiconductor element comprised of at least one individual die location.